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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,149	07/24/2003	Gerald R. Stanley	11336/513 (P03087US)	9305

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EXAMINER	
HAN, YOUNGHUIE JESSICA	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/626,149	STANLEY, GERALD R.
	Examiner	Art Unit
	Y. J. Han	2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39 and 47-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39 and 47-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's request for reconsideration of the restriction requirement of the last Office action is persuasive and, therefore, the restriction requirement of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 34-39, 47-50, and 52-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al (disclosed in IDS filed on 10/31/05) in view of Cyr (5,870,294).

Lai et al discloses the invention substantially as claimed including a first boost converter (Sa1, Da1, C1/Sa2, Da1, C2) that includes a first boost sub-circuit (Sa1, Da1, C1) coupled with a second boost sub-circuit (Sa2, Da1, C2); a second boost converter (Sa3, Da3, C3/Sa4, Da4, C4) coupled in series with the first boost converter, where the second boost converter includes a third boost sub-circuit (Sa3, Da3, C3) coupled with a fourth boost sub-circuit (Sa4, Da4, C4), where the first and second boost converters are configured to receive an input voltage (Vs) and supply a boost voltage (Fig. 1); and Table 1 shows the interleaved phasing such that switching duty of each switch is sequentially phased within a switching cycle; wherein the first and second boost sub-circuits are coupled in series and the third and fourth boost sub-circuits are coupled in series (Fig. 1 shows that all circuits are connected in series); wherein the power factor correction controller is configured to control the first and second boost converters with interleave of at least

four (Table 1 shows interleave of at least four); wherein the each of the first, second, third and fourth boost sub-circuits include a boost switch (Sa1, Sa2, Sa3, Sa4), the boost switch of each of the first, second, third and fourth boost sub-circuits coupled in series and configured to be coupled in parallel with an input voltage; wherein each of the first, second, third and fourth boost sub-circuits include a respective boost switch (Sa1, Sa2, Sa3, Sa4) and a respective boost capacitor (C1, C2, C3, C4), the respective boost capacitor being chargeable by the respective boost switch to a portion of the boost voltage; wherein the first boost converter includes a first boost capacitor (C1) and the second boost converter includes a second boost capacitor (C2), the first and second boost sub-circuits configured to charge the first boost capacitor to a portion of the boost voltage and the third and fourth boost sub-circuits configured to charge the second boost capacitor to a portion of the boost voltage.

Lai et al, however, does not disclose a power factor correction controller configured to control boost converters with pulse modulation. Cyr clearly teaches that the use of such controller is well known in the art. Figure 1 of Cyr shows Power Factor Corrector 22 with a boost topology driven by conditional PWM drive signals output by a gate array logic IC 24. Thus, it would have been obvious to one having ordinary skill in the art to employ the power factor correction controller in Lai et al, as taught by Cyr, to obtain the claimed invention for the purpose of minimizing component stresses.

4. Claims 7-11 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al in view of Cyr, and further in view of Guerrera (5,923,152).

Lai et al as modified by Cyr discloses the invention substantially as claimed but does not disclose boost switches which are independently switchable. Guerrera teaches clearly that the

use of independently controlled switches (40, 46, 80, and 88 in Fig. 5) for obtaining the desired output voltage in the power factor correction circuit is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art to employ independently controlled switches in Lai et al as modified by Cyr, as taught by Guerrera, to obtain the claimed invention for the purpose of achieving highly efficient converter that minimizes harmonics and EMI problems.

5. Claims 12, 19-33, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai et al in view of Cyr, and further in view of Pinheiro et al (disclosed in IDS filed on 03/28/06).

Lai et al as modified by Cyr discloses the invention substantially as claimed but does not disclose converter configured to balance the boost voltage. Pinheiro et al teaches that the use of boost power factor correction configure to balance the boost voltage is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art to employ the balancing of the boost voltage in Lai et al as modified by Cyr, as taught by Pinheiro et al, to obtain the claimed invention for the purpose of achieving highly efficient converter that minimizes input current ripple.

Response to Arguments

6. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Y. J. Han whose telephone number is 571-272-2078. The examiner can normally be reached on Mon-Fri 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

J. Han

J. Han
Primary Examiner
Art Unit 2838